I²C Controlled 13.5V/3A, #1 Cell Battery Charger with Power Path Management and USB Charger Detection

PRELIMINARY DATASHEET

DESCRIPTION

FH56963 is a highly-integrated 3A switch-mode battery charge and system power path management device for single cell Li-ion and Li-polymer battery. It features fast charging with high input voltage support for a wide range of smart phones, tablets and portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life.

Its input voltage and current regulation deliver maximum charging power. The solution is highly integrated with input reverse-blocking FET, high/low-side switching FET, and battery FET. It also integrates the bootstrap diode for the high-side gate drive. The I2C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports a wide range of input sources. The device is compliant with USB 2.0 and USB 3.0 power spec with input current and voltage regulation. The device also meets USB On-the-Go(OTG) operation power rating specification by supplying 5.15V on BUS pin with constant current limit up to 1.2A.

The power path management regulates the system slightly above battery voltage but does not drop below 3.5V minimum system voltage (programmable). With this feature, the system maintains operation even when the battery is completely depleted or removed.

When the input current limit or voltage limit is reached, the power path management automatically reduces the charge current to zero. As the system load continues to increase, the power path discharges the battery until the system power requirement is met. This Supplement Mode prevents overloading the input source.

The FH56963 is available in a QFN4x4-24L package.

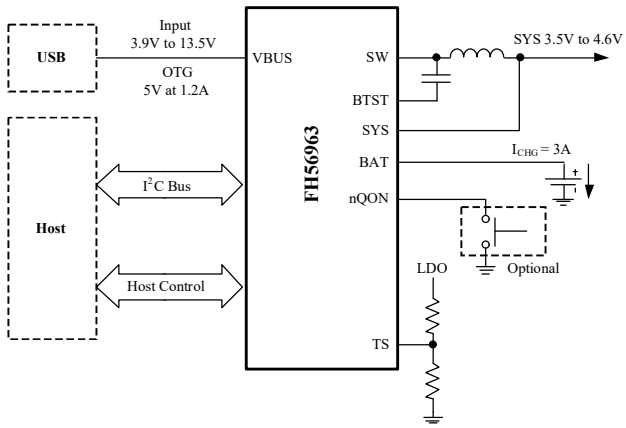
APPLICATIONS

- Tablet PC, Smart Phone, Internet Devices
- Portable Audio Speaker, Handheld Computers, PDA, POS

KEY FEATURES

- High-Efficiency, 1.5MHz, Synchronous Switching Buck Charger
  - 90% Charge Efficiency at 2.0A from 5.0V Input
  - Programmable PFM Mode for Light Load Conditions
- Supports USB On-The-Go (OTG)
  - Programmable Current Limit Boost Converter with Up to 1.2A Output
- Wide Range Single Input to Support both USB Input and High Voltage Adapters
  - Support 3.9V to 13.5V Input Voltage Range With 22V Absolute Maximum Input Voltage Rating
  - Programmable Input Current Limit (100mA to 3.2A With 100mA Resolution)
  - Auto Detect USB BC1.2, SDP, CDP, DCP and Non-Standard Adaptors
- Narrow VDC (NVDC) Power Path Management
- BATFET Control to Support Ship Mode, Wake Up and Full System Reset
- Flexible Autonomous and I²C Mode for Optimal System Performance
- High Integration Includes All MOSFETs, Current Sensing and Loop Compensation
- Safety
  - Battery Temperature Sensing for Charge and Boost Mode
  - Thermal Regulation and Thermal Shutdown
- Input UVLO and Overvoltage Protection

SIMPLIFIED SCHEMATIC



TYPICAL APPLICATION CIRCUIT

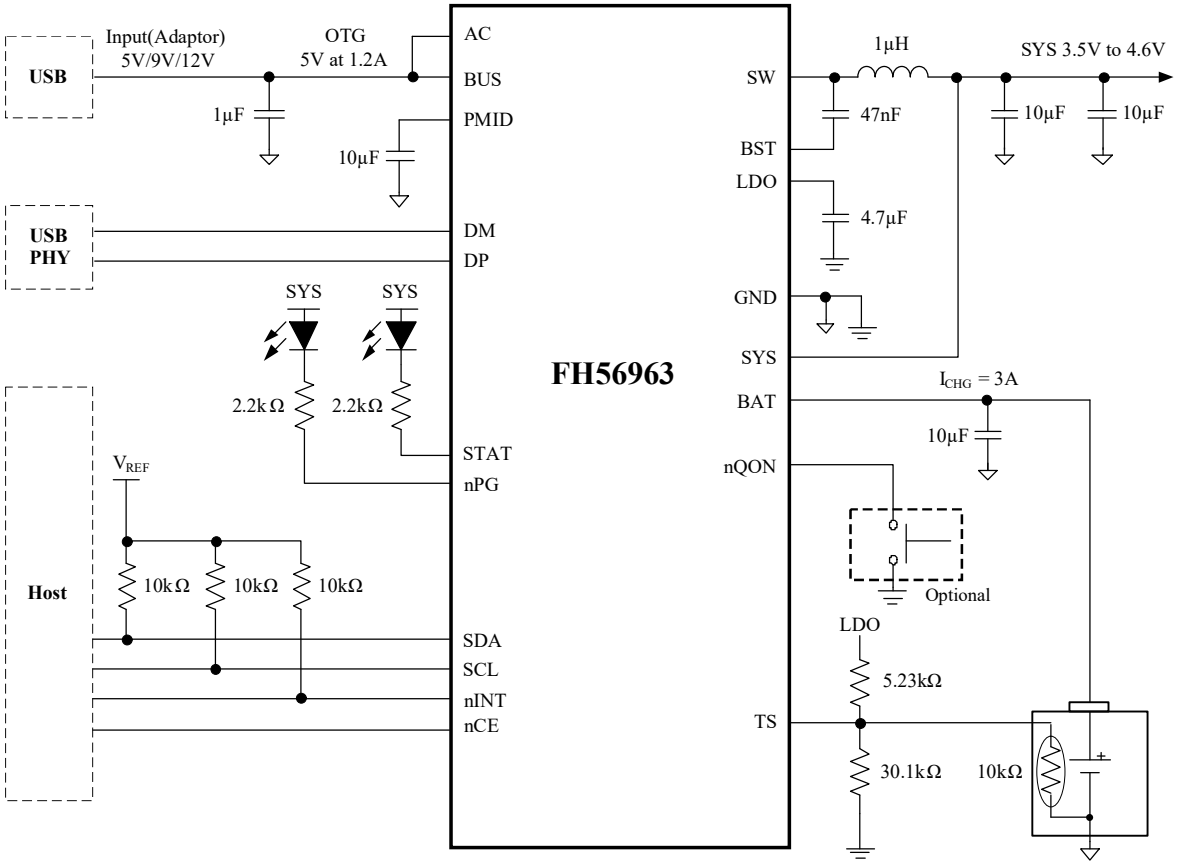
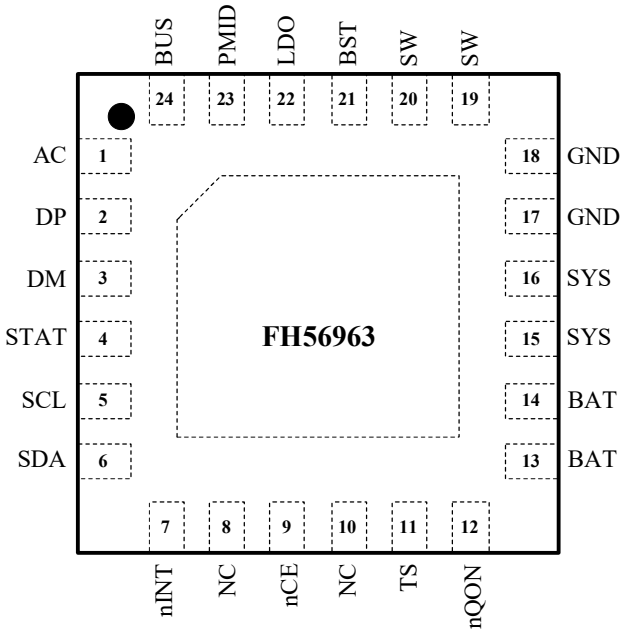


Figure 1. Typical Application Circuit

PIN CONFIGURATION

(TOP VIEW)



QFN4×4-24L

PIN DESCRIPTION

PIN NAME	PIN #	DESCRIPTION
AC	1	Charger input voltage sense. This pin must be connected to BUS pin.
BUS	24	Charger input voltage. Bypass it with a 10uF ceramic capacitor from BUS to PGND. The capacitor should be close to the BUS pin.
DP	2	Positive line of the USB data line pair. DP/DM based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors.
DM	3	Negative line of the USB data line pair. DP/DM based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors
STAT	4	Open-drain charge status output. Connect the STAT pin to a logic rail via 10kΩ resistor. The STAT pin indicates charger status. Connect a current limit resistor and a LED from a rail to this pin. Charge in progress: LOW, Charge complete or charger in SLEEP mode: HIGH. Charge suspend (fault response)or No bat: 1Hz, 50% duty cycle Pulses.
SCL	5	I^2C interface clock. Connect a 10kΩ pull up resistor to the logic rail.
SDA	6	I^2C interface data. Connect a 10kΩ pull up resistor to the logic rail.
nINT	7	Open-drain interrupt Output. Connect the nINT pin to a logic rail through 10kΩ resistor. The nINT pin sends an active low, 256μs pulse to host to report charger device status and fault.
NC	8	No Connect. Keep the pin float
nCE	9	Charge disable control pin. nCE=0, charge is enabled. nCE=1, charge is disabled.
NC	10	No Connect. Keep the pin float
TS	11	Temperature qualification voltage input to support JEITA profile. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from LDO to TS to GND. Charge suspends when either TS pin is out of range. When TS pin is not used, connect a 10kΩ resistor from LDO to TS and connect a 10kΩ resistor from TS to GND. It is recommended to use a 103AT-2 thermistor.
nQON	12	BATFET enable/reset control input. When BATFET is in ship mode, a logic low of $t_{SHIPMODE}$ (typical 1.15s) duration turns on BATFET to exit shipping mode. When V_{BUS} is not plugged-in, a logic low of t_{QON_RST} (minimum 8s) duration resets SYS (system power) by turning BATFET off for t_{BATFET_RST} (minimum 250ms) and then re-enable BATFET to provide full system power reset. The pin contains an internal pull-up to maintain default high logic.
BAT	13, 14	Positive battery terminal. The internal BATFET and current sensing is connected between SYS and BAT. Connect a 10uF close to the BAT pin.
SYS	15, 16	Converter output connection point. The internal current sensing network is connected between SYS and BAT pin. Connect 2x10uF close to the SYS pin.
GND	17, 18	Power Ground
SW	19, 20	Switching node output. Connected to output inductor. Connect the 10nF bootstrap capacitor from SW pin to BST pin.
BST	21	Bootstrap capacitor connection for the high-side FET gate driver. Connect a 10nF ceramic capacitor from BST pin to SW pin.

PIN DESCRIPTION

PIN NAME	PIN #	DESCRIPTION
LDO	22	LDO Output Voltage. Bypass the pin with 4.7μF (10V rating) capacitor from LDO to GND. The capacitor should be closed to the pin.
PMID	23	Connection point between reverse blocking FET and high-side switching FET. Bypass it with 2x10uF capacitor from PMID to PGND. This capacitor should be close to the PMID pin.

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

AC, BUS, PMID pin to GND Voltage ..... -2V to 22V

SW to GND Voltage ..... -0.3V to 22V

SYS, BAT to GND Voltage ..... -0.3V to 6V

BST to SW Voltage ..... -0.3V to 6V

All Other Pin to GND Voltage ..... -0.3V to 6V

SW, BUS, BAT, SYS to PGND current ..... Internally limited

Operating Temperature Range ..... -40°C to 85°C

Storage Temperature Range ..... -55°C to 150°C

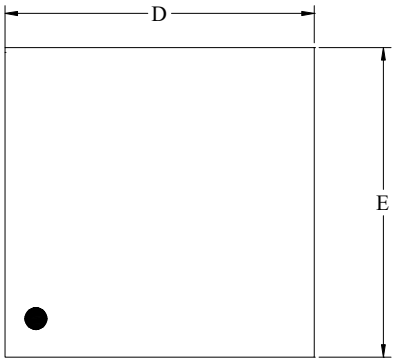
Thermal Resistance	θ_{JA}	θ_{JC}	
QFN4x4-24L	35	10	°C/W

Lead Temperature (Soldering,10sec) ..... 260°C

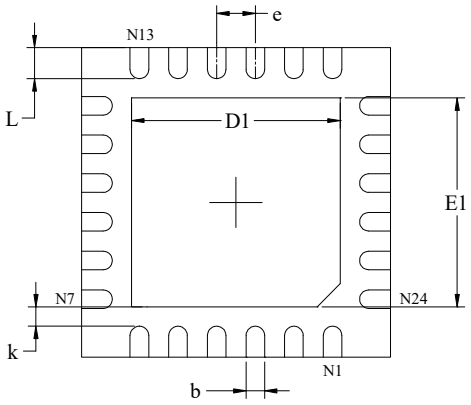
ESD HBM (Human Body Mode) 2KV

PACKAGE OUTLINE DIMENSIONS

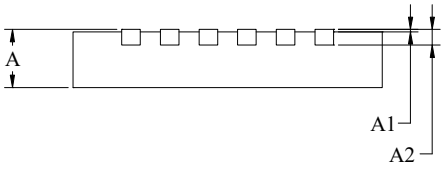
Type: QFN4.0*4.0-24L



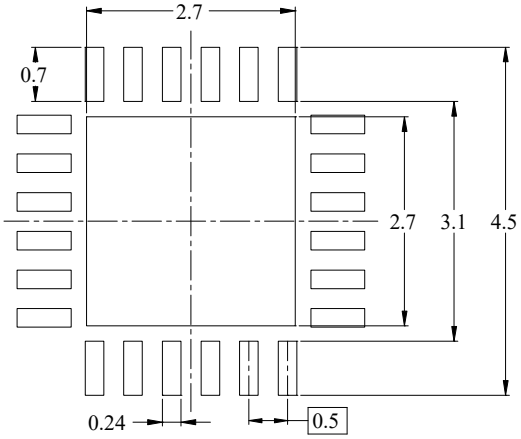
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	3.900	4.100	0.154	0.161
D1	2.600	2.800	0.102	0.110
E	3.900	4.100	0.154	0.161
E1	2.600	2.800	0.102	0.110
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

ORDERING INFORMATION

Part Number	Input Voltage	Features	Operating Temperature	Package Type	Top Mark	SPQ
FH56963D24	~ 22.0V	● Switch boost/boost battery charge ● I2C Controlled ● Frequency: 1.5MHz ● Current limit: 3.2A ● USB OTG, auto detect	-40°C to +85°C	QFN4.0*4.0-24L	FH56963 YY WW LL	5000EA/Reel

Note:

- **FH56963** devices are Pb-free and RoHs compliant.
- The surface prints of our semiconductor devices are subject to change during the production process and do not involve changes in electrical parameters, and we will not separately state the notice.
- If you have any other custom purchase needs, please contact our sales department.
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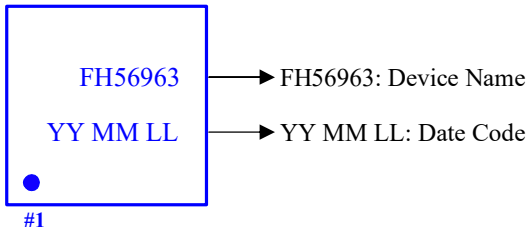
Device Name: DFN4.0x4.0-24L



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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Note:

CAUTION STATIC SENSITIVE DEVICES NOT TO BE HANDLED BY UNAUTHORISED PERSONNEL

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▲ Update by Sep.2022