CMOS General Purpose Timer, 500kHz, 18V

Description

These devices are precision timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the as table mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of VCC. These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit is capable of sinking or sourcing current up to 200mA. Operation is specified for supplies of 2V to 18V. With a 5.0V supply, output levels are compatible with TTL inputs.

Features

- Timing from microseconds to hours
- Astable or mono stable operation
- Adjustable duty cycle
- TTL compatible output can source or sink up to 200mA
- "Green" Molding Compound (No Br, Sb)
- Lead Free Finish/ RoHS Compliant (Note 1)

  Notes: 1. EU Directive 2002/95/EC (RoHS).
  All applicable RoHS exemptions applied.

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector
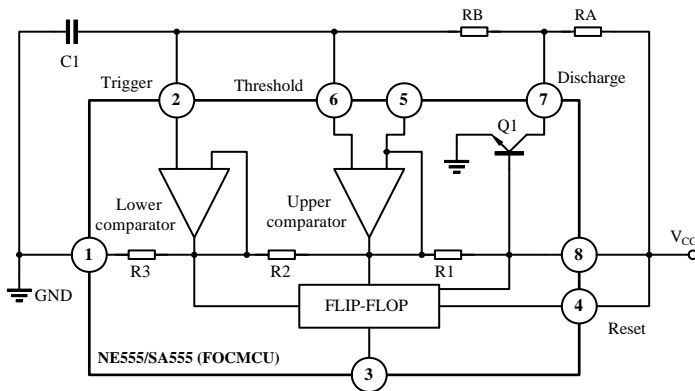
TYPICAL APPLICATION CIRCUIT

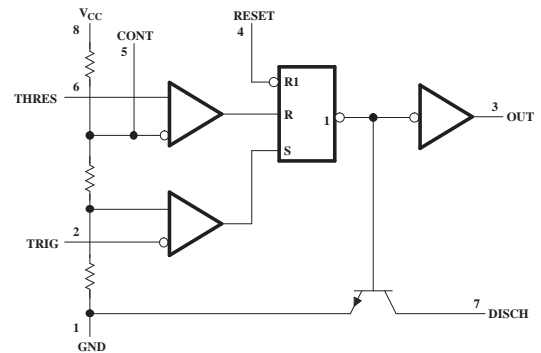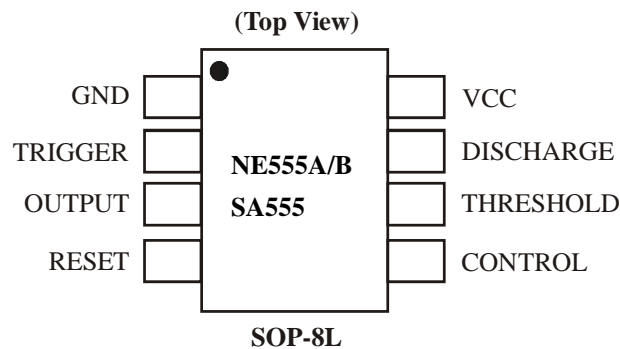**Figure 1. Typical application circuit**

Simplified Schematic

Figure 2. Simplified schematic

Precision Timer ICs

Part Number	Maximum frequency (MHz)	Max output rise time (ns)	Supply current @ VCC = 5V (mA)		VCC min (V)	VCC max (V)	Operating Ambient Temperature Range (°C)	Package Outlines
			Output low	Output high				
NE555A	0.5	300	3	2	2.0	18	0 to 70	SOP-8L
NE555B	0.5	300	3	2	2.0	18	-25 to 85	SOP-8L
SA555	0.5	300	3	2	2.0	18	-40 to 105	SOP-8L

NE555/SA555

Pin Assignments

(Top View)

GND — NE555A/B SA555 — VCC
TRIGGER — — DISCHARGE
OUTPUT — — THRESHOLD
RESET — — CONTROL

SOP-8L

Pin Descriptions

| PIN		I/O	Pin Description
NO.	NAME		
1	GND	In	Ground reference voltage
2	TRIGGER	In	Responsible for transition of the flip-flop from set toreset. The output of the timer depend son the amplitude of the external trigger pulse applied to this pin.
3	OUTPUT	Out	Output driven waveform
4	RESET	Out	Negative pulse applied to this pin to disable or reset the timer. When not used for reset purposes, it should be connected to VCC to avoid false triggering.
5	CONTROL VOLTAGE	In	Controls the threshold and trigger levels. It deter mines the pulse width of the output waveform. An external voltage applied to this pin can also be used to modulate the output waveform.
6	THRESHOLD	In	Compares the voltage applied to the terminal with a reference voltage of 2/3 VCC. The amplitude of voltage applied to this terminal is responsible for the set state of the flip-flop.
7	DISCHARGE	In	Open collect or output which discharges a capacitor between intervals (in phase with output). It toggles the output from high to low when voltage reaches 2/3 of the supply voltage.
8	VCC	In	Supply voltage with respect to GND

APPLICATION CIRCUIT

Oscillator application circuit
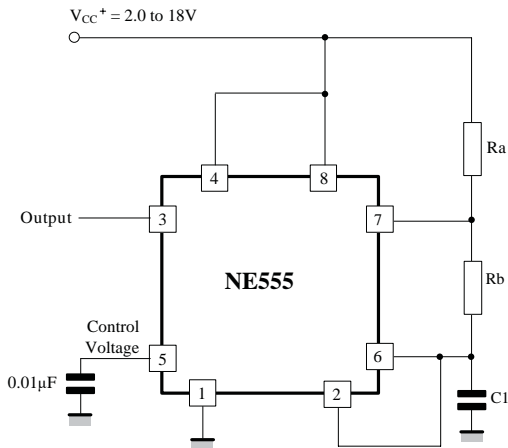
Oscillation period:

$T=0.693(R_A+2R_B)C$ Duty: $D=R_B/(R_A+2R_B)$

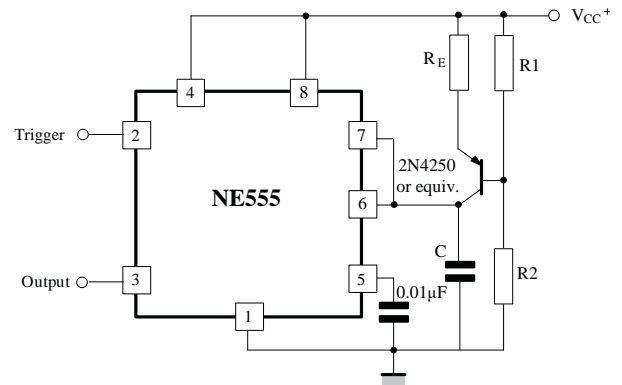### Pulse width modulator
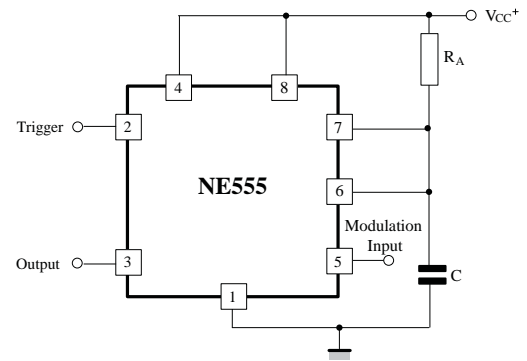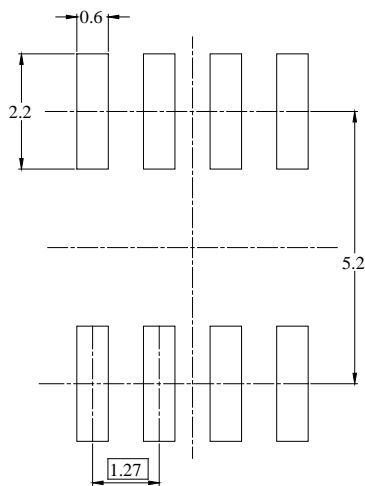

50% duty cycle oscillator

Linear ramp

NE555/SA555
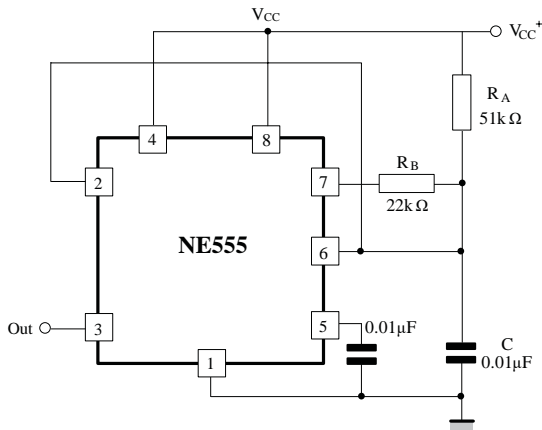
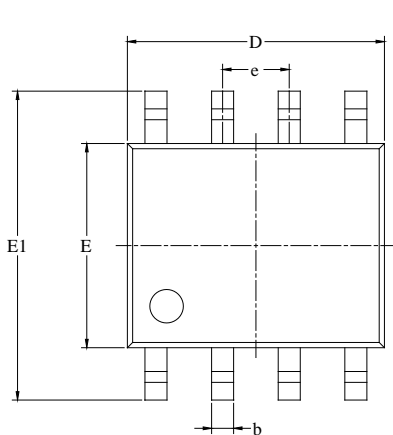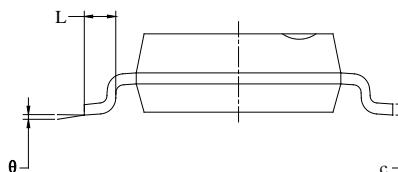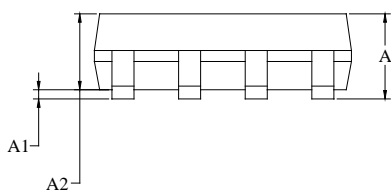## Package Outline Dimensions   (All Dimensions in mm)

Type: SOP-8L

RECOMMENDED LAND PATTERN(Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

ORDERING INFORMATION

| Part Number	Voltage Range	Features	Operating Temperature	Package Type	Top Mark	SPQ
NE555AS8	2.0 ~ 18.0V	● General Purpose Timer ● Input Voltage: ~18.0V ● Max Osc Freq.: 500kHz ● Power Dissipation: 500mW ● Timing Accuracy: 2%	0℃ to +70℃	SOP-8L	NE555A YY MM LL	4000PCS/Reel
NE555BS8	2.0 ~ 18.0V		-25℃ to +85℃	SOP-8L	NE555B YY MM LL	4000PCS/Reel
SA555S8	2.0 ~ 18.0V		-40℃ to +105℃	SOP-8L	SA555 YY MM LL	4000PCS/Reel

Note:

➢ **NE555A/NE555B/SA555** devices are Pb-free and RoHs compliant.

➢ The surface prints of our semiconductor devices are subject to change during the production process and do not involve changes in electrical parameters, and we will not separately state the notice.

➢ If you have any other custom purchase needs, please contact our sales department.

➢ ForDevices reserves the right to amend and legally interpret the electrical parameters of this chip device. (http://www.fordevices.com)

Device Name: SOP-8L

xx555 → NE555A/NE555B/SA555: Device Name

YY MM LL → YY MM LL: Date Code
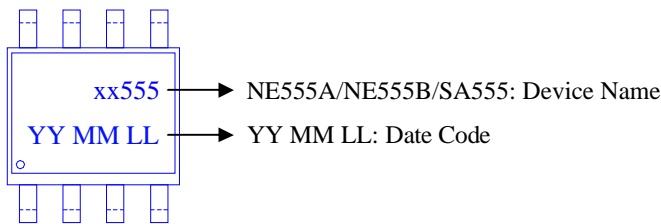
ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.
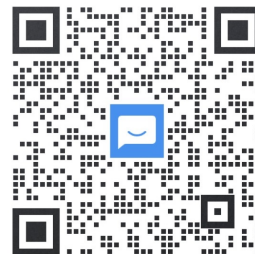
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▲ Update by Feb.2022