Standalone 13.5V/3.0A, #1 Cell Battery Charger with Power Path Management

PRELIMINARY DATASHEET

DESCRIPTION

FH56954 is a highly-integrated 3.0A switch mode battery charge management and system power path management device for single cell Li-ion and Li-polymer battery. It features fast charging with high input voltage support for a wide range of smart phones, tablets and portable devices.

Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. Its input voltage and current regulation deliver maximum charging power to battery.

The solution is highly integrated with input reverse-blocking FET (Q1), high-side switching FET (Q2), low-side switching FET (Q3), and battery FET (Q4) between system and battery. It also integrates the bootstrap diode for the high-side gate drive for simplified system design.

The device supports a wide range of input sources: standard USB host port, USB charging port, and USB compliant high voltage adapter. To support fast charging using high voltage adapter.

The device is compliant with USB 2.0 and USB 3.0 power spec with input current and voltage regulation. The device also meets USB On-the-Go (OTG) operation power rating specification by supplying 5.15V on V_{BUS} with constant current limit up to 1.2A.

The power path management regulates the system slightly above battery voltage but does not drop below 3.50V minimum system voltage. With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the power path management automatically reduces the charge current to zero. As the system load continues to increase, the power path discharges the battery until the system power requirement is met. This Supplement Mode prevents overloading the input source.

FH56954 is available in a QFN4.0*4.0-24L package.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
FH56954	QFN (24L)	4.00mm × 4.00mm

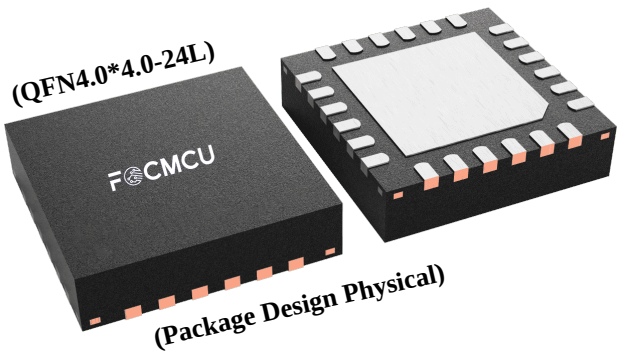
(1) For all available packages, see the orderable addendum at the end of the data sheet.

KEY FEATURES

- 1.5MHz Synchronous Switching Buck Charger
  - 91% Charge Efficiency at 2.0A from 5.0V Input
  - Programmable PFM Mode for Light Load Conditions
- Supports USB On-The-Go (OTG)
  - Boost Converter with Up to 1.2A Output
  - 91% Boost Efficiency at 1.0A Output
  - Output Short Circuit Protection
- Wide Range Single Input to Support both USB Input and High Voltage Adapters
  - Support 3.9V to 13.5V Input Voltage Range with 30.0V Absolute Maximum Input Voltage Rating
  - Maximum Power Tracking by Input Voltage Limit Up to 4.5V (VINDPM)
  - VINDPM Threshold Automatically Tracks Battery Voltage
- High Battery Discharge Efficiency with 27mΩ Battery Discharge MOSFET
- Narrow VDC (NVDC) Power Path Management
- High Integration Includes All MOSFETs, Current Sensing and Loop Compensation
- Safety
  - Battery Temperature Sensing for Charge and Boost Mode
  - Thermal Regulation and Thermal Shutdown
- Input UVLO and Overvoltage Protection
- Available in a QFN4.0*4.0-24L package

APPLICATIONS

- Tablet PC, Smart Phone, Internet Devices
- Portable Audio Speaker
- Handheld Computers, PDA, POS



TYPICAL APPLICATION

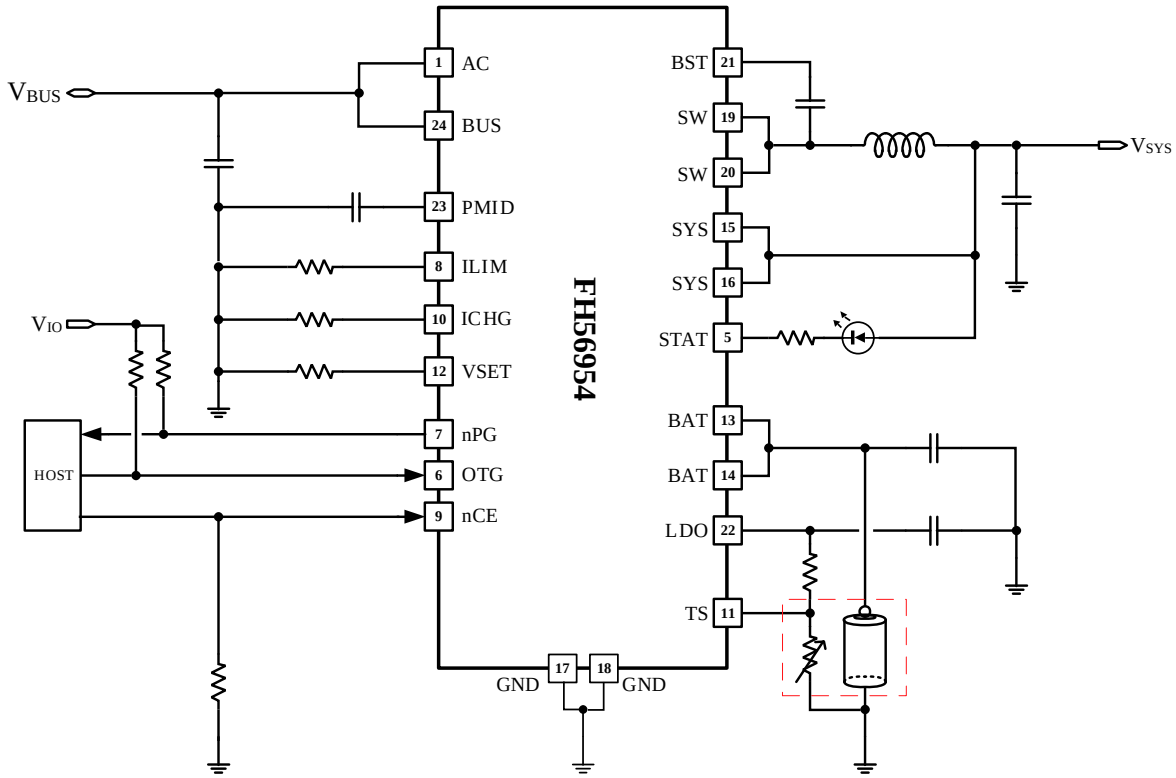
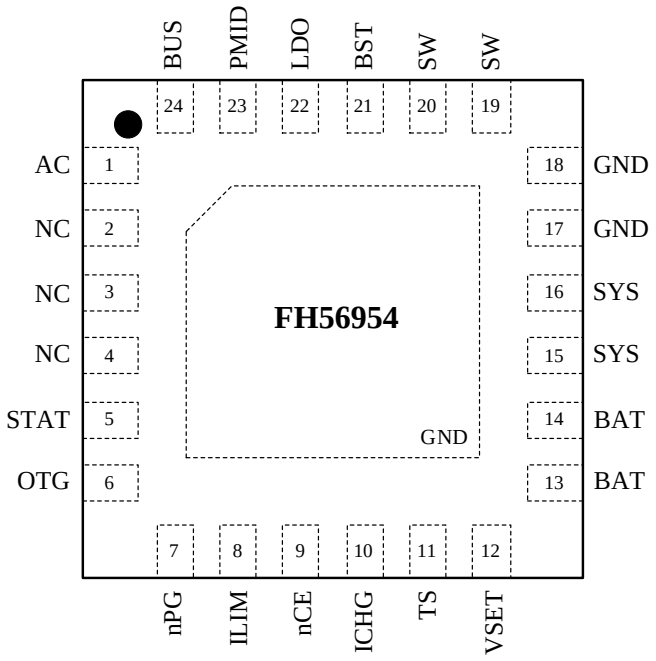


Figure 1. FH56954 Simplified Application

PIN CONFIGURATION

(TOP VIEW)



QFN4.0*4.0-24L

PIN DESCRIPTION

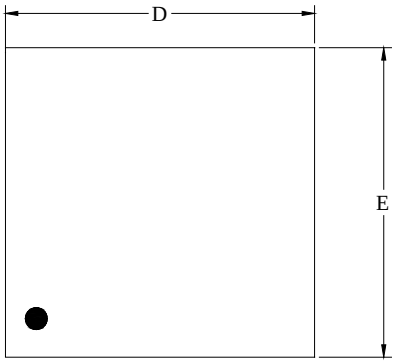
PIN NAME	PIN #	DESCRIPTION
AC	1	Input voltage sensing. this pin must be shorted to BUS pin.
BUS	24	Charger input voltage. Bypass it with a 10uF ceramic capacitor from BUS to PGND. The capacitor should be close to BUS pin.
NC	2	Keep this pin floating, not connected to anything
NC	3	Keep this pin floating, not connected to anything
NC	4	Keep this pin floating, not connected to anything
STAT	5	Open-drain charge status output. Connect the STAT pin to a logic rail via 10kΩ resistor. The STAT pin indicates charger status. Connect a current limit resistor and a LED from a rail to this pin. Charge in progress: LOW, Charge complete or charger in SLEEP mode: HIGH Charge suspend (fault response)or No bat: 1Hz, 50% duty cycle Pulses
OTG	6	Boost mode enable pin. When this pin is pulled HIGH, OTG is enabled. OTG pin cannot be floating.
nPG	7	Open drain active low power good indicator. Connect to the pull up rail through 10kΩ resistor. LOW indicates a good input source if the input voltage is between UVLO and OVP threshold, above SLEEP mode threshold, and current limit is above 30mA.
ILIM	8	ILIM sets the input current limit. A resistor is connected from I_{LIM} pin to ground to set the input current limit as $I_{INDPM} = K_{ILIM} / R_{ILIM}$. The acceptable range for ILIM current is 500mA ~ 3200mA.
nCE	9	Charge disable control pin. nCE=0, charge is enabled. nCE=1, charge is disabled.
ICHG	10	ICHG pin sets the charge current limit. A resistor is connected from ICHG pin to ground to set charge current limit as $I_{CHG} = K_{ICHG} / R_{ICHG}$. The acceptable range for charge current is 300mA ~ 3000mA.
TS	11	Temperature qualification voltage input to support JEITA profile. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from LDO to TS to GND. Charge suspends when either TS pin is out of range. When TS pin is not used, connect a 10kΩ resistor from LDO to TS and connect a 10kΩ resistor from TS to GND. It is recommended to use a 103AT-2 thermistor.
VSET	12	VSET pin sets default battery charge voltage in FH56954. Program battery regulation voltage with a resistor pull-down from VSET to GND. R_{PD} > 50kΩ(float pin) = 4.208V, R_{PD} < 500Ω (short to GND) = 4.352V, 5kΩ < R_{PD} < 25kΩ = 4.400V
BAT	13, 14	Positive battery terminal. The internal BATFET and current sensing is connected between SYS and BAT. Connect a 10uF close to the BAT pin.
SYS	15, 16	Converter output connection point. The internal current sensing network is connected between SYS and BAT. Connect a 3 x 22uF close to the SYS pin.

PIN DESCRIPTION

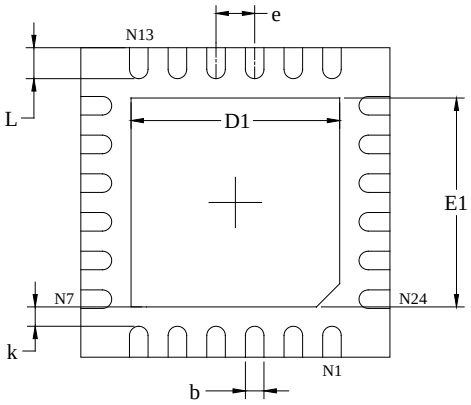
PIN NAME	PIN #	DESCRIPTION
GND	17, 18	Power Ground
SW	19, 20	Switching node output. Connected to output inductor. Connect the 10nF bootstrap capacitor from SW to BST.
BST	21	Bootstrap capacitor connection for the high-side FET gate driver. Connect a 10nF ceramic capacitor from BST pin to SW pin.
LDO	22	LDO Output Voltage. Bypass the pin with 4.7uF capacitor from LDO to GND. The capacitor should be closed to the pin.
PMID	23	Connection point between reverse blocking FET and high-side switching FET. Bypass it with a minimum of 10uF capacitor from PMID to PGND. This capacitor should be close to the PMID pin.
EP	EP	Thermal pad and ground reference. This pad is ground reference for the device and it is also the thermal pad used to conduct heat from the device. This pad should be tied externally to a ground plane through PCB vias under the pad.

PACKAGE OUTLINE DIMENSIONS

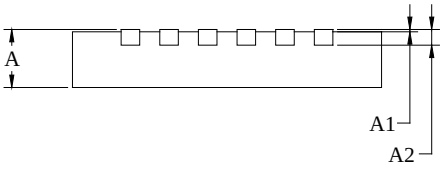
Type: QFN4.0*4.0-24L



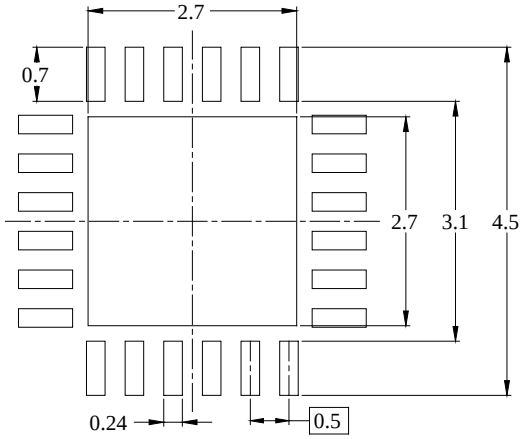
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	3.900	4.100	0.154	0.161
D1	2.600	2.800	0.102	0.110
E	3.900	4.100	0.154	0.161
E1	2.600	2.800	0.102	0.110
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

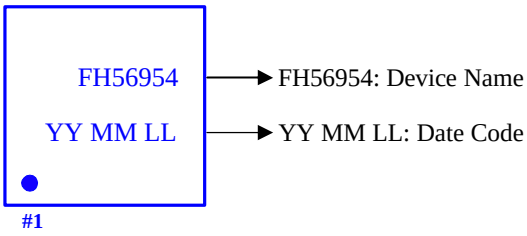
ORDERING INFORMATION

Part Number	Input Voltage	Features	Operating Temperature	Package Type	Top Mark	SPQ
FH56954D24	~ 30.0V	● Switch boost/boost battery charge ● I2C Controlled ● Frequency: 1.5MHz ● Current limit: 3.2A ● USB OTG, auto detect ● NVDC Power Path Management	-40℃ to +85℃	QFN4.0*4.0-24L	FH56954 YY WW LL	5000EA/Reel

Note:

- **FH56954** devices are Pb-free and RoHs compliant.
- The surface prints of our semiconductor devices are subject to change during the production process and do not involve changes in electrical parameters, and we will not separately state the notice.
- If you have any other custom purchase needs, please contact our sales department.
- FOCMCU Inc. reserves the right to amend and legally interpret the electrical parameters of this chip device. (http://www.fordevices.com)

Device Name: DFN4.0x4.0-24L



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Product Folder | Order Now | Technical Documents | Tools & Software | Support & Community

Note:

- The information described herein is subject to change without notice.
- FOCMCU Inc. is not responsible for any problems caused by circuits or diagrams described herein whose related industrial properties, patents, or other rights belong to third parties. The application circuit examples explain typical applications of the products, and do not guarantee the success of any specific mass-production design.
- Use of the information described herein for other purposes and/or reproduction or copying without the express permission of FOCMCU Inc. is strictly prohibited.
- The products described herein cannot be used as part of any device or equipment affecting the human body, such as exercise equipment, medical equipment, security systems, gas equipment, or any apparatus installed in airplanes and other vehicles, without prior written permission of FOCMCU Inc.
- Although FOCMCU Inc. exerts the greatest possible effort to ensure high quality and reliability, the failure or malfunction of semiconductor products may occur. The user of these products should therefore give thorough consideration to safety design, including redundancy, fire-prevention measures, and malfunction prevention, to prevent any accidents, fires, or community damage that may ensue.

▲ Update by Nov.2022